REMARKS/ARGUMENTS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1, 2, and 4-25 are pending in the present application. Claim 3 has been canceled without prejudice or disclaimer. Claims 1, 6-9, 13-16, and 21 have been amended by the present amendment and new Claims 22-25 have been added without the introduction of any new matter. In this regard note the input to the common gate between 122 and 123 of FIG. 13 is supplied from the common node between the outputs of 101b and 102b that exemplify charge and discharge type squaring circuits. Further note the common gate between 122 and 123 is provided at the output of 116 that has inputs connected to 101 and 102 in FIG4, for example. Note also the showings of FIGS. 16 and 18-19 that also have the same output stage.

The outstanding Action, Claims 6-8 and 13-15 were rejected under the second paragraph of 35 U.S.C. §112; Claims 1, 2, 6-10, and 13-20 were rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 6,204,719 to Gilbert; and Claims 4, 5, 11, 12, and 20 were rejected under under 35 U.S.C. §103(a) as unpatentable over Gilbert in view of U.S. Patent No. 6,563,319 to Kraz.

Initially it is noted that no objection or rejection statement was offered in the outstanding Action as to Claim 21 added by the last amendment. However, page 4 of the outstand ing Action appears to present reasoning for a rejection without the required rejection statement setting forth the grounds relied on. Clarification as to the status of Claim 21 is believed to be in order.

Turning to the stated rejection of Claims 6-8 and 13-15 under the second paragraph of 35 U.S.C. §112, it appears that the focus of the rejection is on the term "comparison circuit"

in Claims 6 and 13 and the fact that this term was used at page 11 of the specification to describe a "differential amplifier 116" that is shown in FIGS. 4, 18, and 19, for example, but not in FIGS. 13 and 16 for example. However, this problem has been eliminated by the present rewording of Claims 6 and 13 and their parent Claims 1 and 9. Consequently, it is now believed to be clear that parent Claims 1 and 9 present limitations readable on all of these Figures that have the same output stage but different input configurations to supply the common gate of the output stage shown between 122 and 123 in all of these Figures, for example. Clearly, both FIGS. 13 and 16 illustrate the connection node directly connecting an output terminal of the first voltage/current conversion circuit (101b,c, for example) and an output terminal of the second voltage/current conversion circuit (102b,c, for example) to the common gate (between 122, 123, for example), and a capacitor connected between the connection node and a ground potential. Accordingly, withdrawal of this rejection is respectfully requested.

The stated rejection of Claims 1, 2, 6-10, and 13-20 under 35 U.S.C. §102(b) as being anticipated by Gilbert notes reliance on the showing of FIG. 4 as to combining two voltage/current conversion circuits (13,15) with circuit 18A, and noting that 18A has an output node as to Claims 6 and 13. The outstanding Action further notes that Gilbert discloses a configuration (FIG. 2) that includes combining a signal level detector (12, 14, 16, 18) with an amplification circuit (26) with reference to Claims 16-19.

However, Claims 1, 2, and 4-25 now all include a recitation of the output stage requiring that this stage include a common gate connected to the input that is receiving signals from the voltage/current conversion circuits, subject matter not taught or suggested by Gilbert.

Accordingly, the withdrawal of the rejection of Claims 1, 2, 6-10, and 13-20 under 35 U.S.C. §102(b) as being anticipated by Gilbert is respectfully requested.

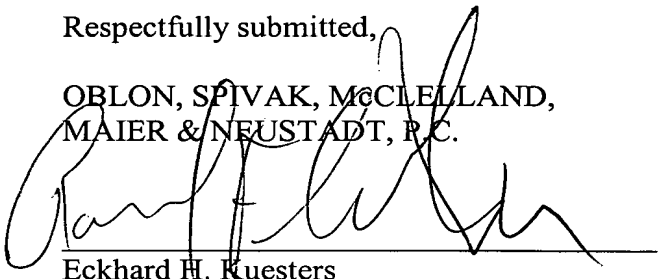
As Kraz does not correct the deficiencies noted as to Gilbert, and as Claims 4, 5, 11, 12, and 20 all include the required output stage and common gate connection by virtue of dependency on either Claim 1,9, or 16, the rejection of Claims 4, 5, 11, 12, and 20 under under 35 U.S.C. §103(a) as unpatentable over Gilbert in view of Kraz is traversed for the reasons noted above.

New Claims 22-25 are even more detailed as to the contents of the above-noted output stage and set forth that it has two constant current sources connected in series with the pMOSFET and nMOSFET that include the common gate. This claimed output stage is what provides the control signal (CNT, for example). Gilbert and Kraz includes no teachings or suggestions of such subject matter such that it is submitted that Claioms 22-25 are clearly patentable over these references.

Consequently, in light of the above discussion and in view of the present amendment, the present application is believed to be in condition for formal allowance and an early and favorable action to that effect is, therefore, respectfully requested.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.



Eckhard H. Kuesters
Attorney of Record
Registration No. 28,870
Raymond F. Cardillo, Jr.
Registration No. 40,440

Customer Number
22850

Tel: (703) 413-3000
Fax: (703) 413 -2220
(OSMMN 06/04)

EHK:RFC:jmp